IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

VIASAT, INC., **Plaintiff,** **vs.** **KIOXIA CORPORATION and KIOXIA AMERICA, INC.,** **Defendants.**	**Case No. 6:21-cv-1231**

DEFENDANT'S MOTION TO DISMISS PURSUANT TO RULE 12(b)(6)

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I. INTRODUCTION

This Court should dismiss the complaint filed by the Plaintiff, Viasat, LLC ("ViaSat"), because it fails to plausibly state a claim that Defendants, Kioxia Corporation and Kioxia America, Inc. (collectively "Kioxia"), infringe ViaSat's patent.[1] *See Ashcroft v. Iqbal*, 556 U.S. 662 (2009). The asserted claims of U.S. Patent No. 8,615,700 (the "'700 Patent"), the single patent at issue, recite systems and methods for detecting and correcting errors in data read from flash memory. Flash memory, such as NAND flash, stores information as electrical charges in transistors. Despite its other improvements over previous memory systems, flash memory becomes increasingly error prone as a function of transistor age, density, and frequency of use.

The '700 Patent describes a modular system for addressing errors in flash memory data. '700 Patent, Abstract. The disclosed system reads encoded data from flash memory into a decoding module, which decodes it to generate a plurality of partially decoded data streams. *Id.* at 10:47-51. Those streams are then sent to parallel error detecting modules. *Id.* at 10:52-59. If errors are detected, the data containing errors is forwarded to a physically separate error correcting module. *Id.* at 10:60-65.

ViaSat concedes that error correction systems for flash memory existed before filing its patent. *See* ECF No. 1 ("Compl.") ¶ 35. As ViaSat conceded during prosecution, earlier systems corrected errors by demodulating data read from flash memory in a decoding module, detecting errors therein with an error detection module, and correcting those errors once detected. *See* Ex. A, Excerpts from the Prosecution History of the '700 Patent, at 9-12.[2] According to ViaSat, the

[1] ViaSat mentions "indirect" infringement in paragraph 8 and in its Prayer for Relief § A. However, in its allegations, Compl. ¶¶ 53-62, ViaSat specifies that its infringement claim is under 35 U.S.C. § 271(a), which only encompasses direct infringement. ViaSat has not provided any factual allegations relevant to the requirements for indirect infringement. See Compl. ¶ 54.

[2] An asserted patent's prosecution history is considered for purposes of testing the complaint under Rule 12(b)(6). *See Data Engine Techs. LLC v. Google LLC*, 906 F.3d 999, 1008 (Fed. Cir. 2018)

inventive contributions in the '700 Patent relate to: (1) decoding data to generate a plurality of partially decoded data streams; (2) detecting errors in a plurality of parallel error detection sub-modules, and (3) physically separating error detection from error correction. *See* Compl. ¶ 39; *see also* '700 Patent, Claim 1 at 10:47-65 *and* Ex. A at 10-12.

ViaSat's implausible allegations that Kioxia's NAND flash-memory products infringe these purported inventive contributions are deficient and self-contradicting. The complaint all but ignores the requirement that error detection and correction be physically separated. Indeed, the *only* affirmative facts ViaSat puts forward to show a plurality of parallel error detector modules in Kioxia's products run squarely against the physical separation limitation, making infringement implausible on its face.

In addition, ViaSat's complex claimed technology requires a heightened level of detail when pleading infringement of claim limitations that are directed to points of novelty. However, ViaSat glosses over those very claim elements with even weaker factual allegations than it uses to support other distinct and independent claim limitations.

Because of these contradictions and deficiencies, described more fully below, the Court should dismiss ViaSat's claim that Kioxia infringes the '700 Patent.

II. BACKGROUND

The '700 Patent teaches systems and methods for error detection and correction through a series of modules that can be implemented in hardware, software, firmware, and the like. Several required limitations set forth in Claim 1 are shown below:[3]

- "a decoding module configured to: **receive encoded data from the flash memory**;" '700 Patent, Claim 1 at 10:48-49 (emphasis added) (hereafter referred

[3] ViaSat only includes allegations for Claim 1. See Compl. ¶ 55.

to as the "received data" limitation); and

- "**decode the received encoded data to generate a plurality of partially decoded data streams**" *Id.* at 10:50-51 (emphasis added) (hereafter referred to as the "decoding data" limitation);

- "**an error detection module** . . . **comprising a plurality of error detection sub-modules operating in parallel**," *Id.* at 10:52-54 (emphasis added) (hereafter referred to as the "plural parallel detectors" limitation); and
- an "**error correction module**, communicatively coupled with and **physically separate from the error detection module** . . . ." *Id.* at 10:62-64 (emphasis added) (hereafter referred to as the "physical separation" limitation).

As the specification describes, and as ViaSat argued during prosecution, the "decoding data" limitation requires that the decoding module do more than simply pass a received stream of data through without modification. *See id.* at 6:11-14, 10:50-51; *see also* Ex. A at 10 (distinguishing from a prior art reference by arguing that the reference discloses "demodulating versus the claimed decoding," and that the decoding module outputs "only a single stream . . . versus the claimed plurality of streams") (emphasis in original). ViaSat also identified the claims' requirements of "plural parallel detectors" and "physical separation" of the modules as points of novelty during prosecution and touted the same in its complaint. *See* Ex. A at 10-12; *see also* Compl. ¶ 39.

III. ARGUMENT

Rule 12(b)(6) authorizes the court to dismiss a complaint that does not include "enough factual matter" that, when accepted as true, "state a claim to relief that is plausible on its face." *Ashcroft v. Iqbal*, 556 U.S. 662, 663 (2009) (quoting *Bell Atl. Corp. v. Twombly*, 550 U.S. 544,

547 (2007)); *see also id.* at 678 (ruling that the plausibility standard is only met where "factual content . . . allows the court to draw the reasonable inference" of the defendant's liability) *and* FED. R. CIV. P. 12(b)(6). "[T]hreadbare recitals of a cause of action's elements, supported by mere conclusory statements" are insufficient, as courts "are not bound to accept as true [] legal conclusion[s] couched as [] factual allegation[s]." *Iqbal*, 556 U.S. at 678-79. In patent infringement actions, this means that the plaintiff must do more than "recit[e] the claim elements and merely conclud[e] that the accused product has those elements." *Bot M8 LLC v. Sony Corp. of Am.*, 4 F.4th 1342, 1353 (Fed. Cir. 2021). While a plaintiff need not "plead facts establishing that each element of an asserted claim is met," the "failure to allege facts that plausibly suggest a specific element or elements of a claim have been practiced may be fatal in the context of a motion to dismiss." *In re Bill of Lading Transmission & Processing Sys. Pat. Litig.*, 681 F.3d 1323, 1334-35 (Fed. Cir. 2012). Further, dismissal is warranted where "the factual allegations are actually inconsistent with and contradict infringement." *Bot M8*, 4 F.4th at 1354. And when assessing a motion to dismiss, the Court may properly consider the prosecution history of the patent(s) at issue. *See Vervain, LLC v. Micron Tech., Inc.*, No. 6:21-CV-00487-ADA, 2022 WL 23469, at *5 n.2 (W.D. Tex. Jan. 3, 2022) (Albright, J.) ("Courts may take judicial notice of government records, like prosecution history available on the U.S. Patent & Trademark Office's Public PAIR site, even when resolving a Rule 12(b)(6) motion.").

The Federal Circuit employs a "flexible inquiry" into the sufficiency of factual allegations, where "[t]he level of detail required . . . depends on multiple factors, not limited to 'the complexity of the technology, the materiality of any given element to practicing the asserted claim(s), and the nature of the allegedly infringing device.'" *Vervain*, 2022 WL 23469 at *2 (quoting *Bot M8*, 4 F.4th at 1353). Indeed, this Court made clear that "a higher level of detail in pleading infringement

may – depending on the complexity of the technology – be demanded for elements clearly 'material' to novelty and non-obviousness." *Id.* at *5. "Factual content, not just conclusory allegations" is required for pleading "under any standard," but the heightened standard under *Bot M8* requires more. *Id.* at *2. However, its specific requirements depend on context. *See Bot M8*, 4 F.4th at 1353; *see also Iqbal*, 556 U.S. at 663–64 ("[D]etermining whether a complaint states a plausible claim is context specific, requiring the reviewing court to draw on its experience and common sense.").

A. ViaSat's Complaint Should Be Dismissed Because it is Inconsistent and Insufficiently Pled

ViaSat's complaint fails because it rarely alleges anything beyond bald claim recitations, and when it does, it steps directly into a fatal inconsistency. Failing to meet its pleading requirements, ViaSat puts nothing forward beyond parroted claim language to allege that Kioxia's products include the "physical separation" limitation. The pleading is insufficient based on this deficiency alone. However, ViaSat pushes towards dismissal even further by attempting to show the presence of the "plural parallel *detectors*" limitation solely with allegations directed towards error *correction* functionality. This flatly contradicts the "physical separation" limitation and independently merits dismissal.

Moreover, ViaSat's claimed technology is complex enough to require a heightened level of detail in pleading infringement of material claim limitations. Yet, ViaSat leaves those critical limitations starved of factual support. Aside from abandoning the material "physical separation" requirement, ViaSat copies *one* timing diagram, unlabeled as to its probe location, to allege the presence of *three* distinct limitations concerning different modules in the claimed circuit, two of which were emphasized by Viasat itself during prosecution as points of novelty. Indeed, because these three limitations perform mutually exclusive operations, it is not possible for one single

timing diagram reflecting one single probing location to show the presence of all three limitations. Dismissal is warranted in either case.

1. ViaSat's Complaint is Inconsistent with Infringement

To infringe any claim of the '700 Patent, the accused product must perform, *inter alia*, the "plural parallel detectors" and "physical separation" limitations. *See* '700 Patent, Claim 1 at 10:52-64, Claim 15 at 12:27-30, *and* Claim 17 at 12:52-61. These two essential limitations are illustrated in Figure 3 of the '700 Patent, provided below with annotations:

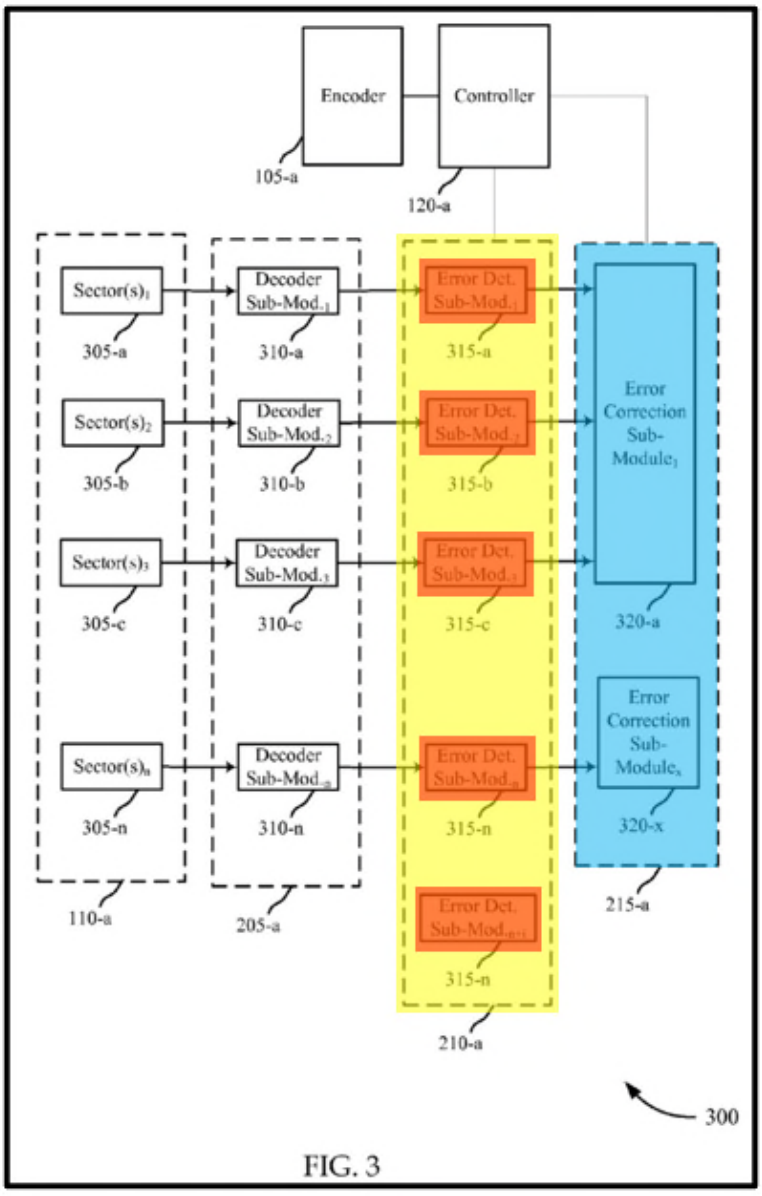


FIG. 3

'700 Patent fig. 3 (annotated). As shown, the claimed flash memory decoder has a detector module 210-a (yellow) comprising multiple parallel detector sub-modules 315-a through 315-n (orange) that are physically separate from the error correction module 215-a (blue).

ViaSat publicly highlighted the importance of the "plural parallel detectors" and "physical separation" limitations on at least two separate occasions. Specifically, during prosecution, ViaSat overcame a prior art reference ("Suzuki") by arguing that Suzuki did not teach "a plurality of error detection sub-modules operating in parallel" and did not teach that the "plurality of error detection sub-modules operating in parallel" and "error correction module" are "physically separate." Ex. A at 10-12.

Notably, in the prosecution history ViaSat unequivocally stated that "the claimed error detection module comprises a plurality of error detection sub-modules performing the same functions and operating in parallel, whereas in Suzuki, the various functional blocks . . . perform different functions and operate serially." Ex. A at 11 (emphasis in original). Later, in similar underscored fashion, ViaSat distinguished Suzuki again by stating that "the claimed error correction module is physically separate from the claimed error detection module, but the cited portions of Suzuki teach conventional . . . decoding, wherein error detection and error correction . . . is not performed by modules which are physically separate." Ex. A at 11-12 (emphasis in original). In its complaint, ViaSat also specifically characterized the "plural parallel detectors" and "physical separation" limitations as being "[u]nlike previous systems." *See* Compl. ¶ 39.

Accordingly, the '700 Patent, the prosecution history, and ViaSat's own complaint confirm that for a product to infringe, it must have an error detection module with multiple sub-modules in parallel, and that error detection circuitry cannot be physically combined with error correction circuitry.

Despite these repeated emphases, ViaSat leaves the "physical separation" limitation completely unsupported. After touting the purported inventiveness of the "physical separation" limitation, ViaSat attempts to prop it up with absolutely nothing other than restated claim language. *See* Compl. ¶ 62.

Further, the only affirmative facts that ViaSat actually puts forward to allege satisfaction of the "plural parallel ***detectors***" limitation are (1) an unintelligible timing diagram, discussed *infra* (Section III.A.2.b); and (2) the following quote: "Kioxia has described its QSBC error correction as including 'multiple error ***correction circuits*** that can select the most efficient error correction operation for different level errors . . . .'" Compl. ¶¶ 60 – 61 (emphasis added).

To the extent ViaSat argues that the quoted language disclosing "multiple error ***correction*** circuits" shows that Kioxia's products have multiple error ***detection*** sub-modules arranged in parallel, ViaSat effectively relies on the "multiple error *correction* circuits" being the same as the error *detection* sub-modules, which flatly contradicts both the claim language and ViaSat's own statements. *Id.* (emphasis added). To be sure, ViaSat point blank states in its complaint that the operation of Kioxia's "multiple ***correction circuits*** . . . ***involves the detection of errors*** by an error detection module" without any evidence, or even suggestion that the detection module is physically separate from the correction circuitry. Compl. ¶ 60 (emphasis added).

Yet, as ViaSat pointed out during prosecution and in its complaint, having the same circuitry perform error detection and correction runs afoul of the "physical separation" limitation. *See* Ex. A at 10-11; *see also* Compl. ¶ 39. This is flatly "inconsistent with and contradict[s]" the claim limitations that were argued for during prosecution, and as such is "insufficient to state a plausible claim." *See Bot M8*, 4 F.4th at 1354; *see also id.* at 1346 ("[A] patentee may subject its

claims to early dismissal by pleading facts that are inconsistent with the requirements of its claims.").

2. ViaSat's Complaint Has Insufficient Factual Matter

Independently, there is insufficient factual matter alleged in the complaint to meet any pleading standard, much less the heightened pleading standard under *Bot M8*. *See Bot M8*, 4 F.4th at 1353. A higher level of detail in pleading is required where (1) "the technology is not simple;" and (2) "the limitations-at-issue are material." *Vervain*, 2022 WL 23469 at *5. The technology, materiality, and factual insufficiency issues here are strikingly similar to *Vervain*, and like *Vervain*, this case involves specific configurations of circuitry. *Id.* Accordingly, this Court should, as it did in *Vervain*, "demand a higher level of pleading." *Id.* The scant factual material in ViaSat's complaint is not enough to overcome that heightened pleading requirement.

a. The Court Should Require A Higher Level of Pleading Detail Because the Technology is Complex and the Limitations-at-issue Are Material

In *Vervain*, this Court applied the higher pleading requirement after finding that technology relating to "software and firmware for using solid-state memory" was "no less complex than that in *Bot M8*." *Id.*; *see also Bot M8*, 4 F.4th 1342 (granting dismissal where technology at issue related to game and authentication programs being stored in memory). The technology in *Vervain* related specifically to data management techniques for information stored in NAND flash memory systems. *See Vervain*, 2022 WL 23469 at *1. The technology at issue here similarly deals with error detection and correction techniques for data stored in NAND flash memory systems that "may be implemented in . . . software [and] firmware . . . ." '700 Patent at 10:26-28. ViaSat's claimed technology is therefore no less complex than that in *Vervain*. 2022 WL 23469, at *5.

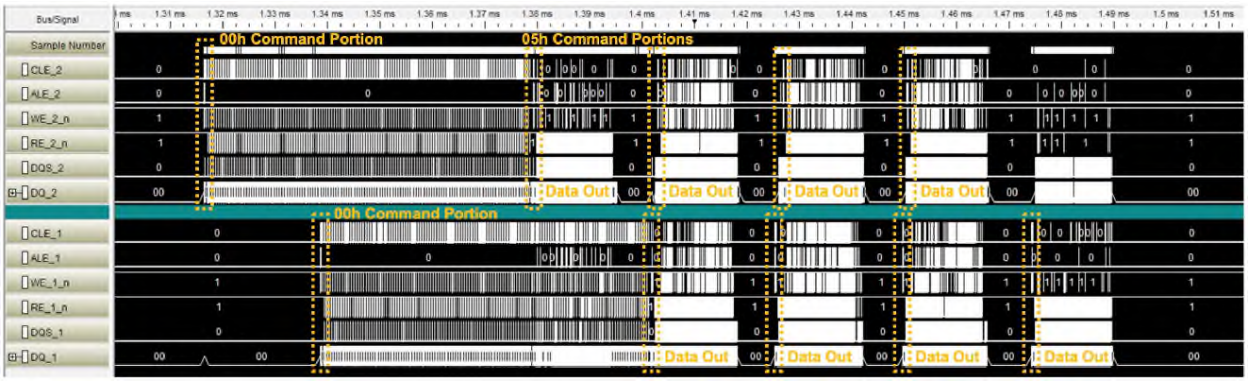
The "decoding data" and "plural parallel detectors" limitations require more detailed pleading than what ViaSat provided because all three are admittedly material. For the purposes of

literal infringement, every claim element is "material" in the sense that "each and every limitation set forth in a claim [must] appear in an accused product." *Id.* (citing to *V-Formation, Inc. v. Benetton Grp. SpA*, 401 F.3d 1307, 1312 (Fed. Cir. 2005)). But for the purposes of determining whether the heightened pleading standard applies, a claim element is "material" if it specifically goes "to novelty and non-obviousness." *Vervain*, 2022 WL 23469 at *5. As discussed *supra* (Sections II and III.A.1), ViaSat repeatedly underscored these limitations to distinguish prior art during prosecution, Ex. A at 9-12, and expressly conceded the materiality of "plural parallel detectors" in its complaint with such clarity that it bears repeating: "[u]nlike previous systems, the '700 Patent claims an error-correction architecture that . . . parallelized error detection." Compl. ¶ 39 (emphasis added). The prosecution history and the complaint show that these limitations are VaiSat's alleged point of novelty, and they are therefore material. As such, in light of the complexity and materiality, these limitations require a heightened level of detail in pleading.

b. ViaSat's Factual Allegations are Insufficient Under the Appropriate Pleading Requirement

ViaSat's factual allegations are insufficient under the heightened pleading requirement appropriate for the technology because the same narrow assertions are offered repeatedly to show that several distinct and independent claim limitations are present. The facts put forward are insufficient to show the "decoding data" and "plural parallel detectors" limitations. Moreover, rehashing those same facts to support additional limitations only illuminates the insufficiency of the complaint.

Specifically, ViaSat uses copies of the exact same timing diagram when it claims to show the presence of the "received data" limitation, as well as the material "decoding data" and "plural parallel detectors" limitations. The copied timing diagram is reproduced below:



Compl. ¶ 51, 59, and 61. Viasat does not offer any information about what portion of what circuit is being analyzed, when, or for what operation.

Rather, ViaSat merely alleges, without evidence, that the diagram illustrates the output characteristics of an alleged decoder, which is not shown, stating that the "decoder splits [] data into discrete packages."[4] Compl. ¶ 51. Later, ViaSat copies the same diagram to show encoded output characteristics of a flash memory chip. Compl. ¶ 59 (alleging that the diagram shows that "the data transferred from the flash memory occurs in discrete units with data, metadata, and ECC check bytes that are subsequently decoded") (emphasis added). Finally, ViaSat copies the same diagram again, this time to implausibly allege that it is evidence of "a plurality of error detection sub-modules operating in parallel, each error detection sub-module configured to: receive a different one of the plurality of partially decoded data streams." Compl. ¶ 61 (alleging that the

[4] ViaSat never actually identifies a decoder in Kioxia's products. Instead, ViaSat points to a photograph of a circuit with a flash memory module and a "controller" chip, each made up of millions of nanometer-wide transistors and alleges that a decoder is included in the "controller" chip. *See* Compl. ¶ 50. This same "controller" chip is alleged to include the detector module, its alleged sub-modules, and the corrector module, none of which are visible from the photograph. *See* Compl. ¶¶ 50, 52, 57, 59, and 60-62.

"multiple data streams . . . upon information and belief . . . each enter error-detection sub-modules."); *see also supra* Section III.A.1.

ViaSat's repeated use of the same single timing diagram for disparate claim limitations confirms the insufficiency of its allegations. One diagram showing electrical 0s and 1s measured over time at some unspecified point in an unspecified circuit merely identifies a digital operation, nothing else. For example, if ViaSat's assertion that the timing diagram shows encoded flash memory output is assumed to be true, then that same diagram cannot also be assumed to show decoded output from the decoder, or input to the "plural parallel detectors" unless the decoder performs no function on the data at all.[5] And such is expressly prohibited by the "decoding data" limitation. *See* '700 Patent, Claim 1 at 10:48-51 (claiming "a decoding module configured to: receive encoded data from the flash memory; and decode the received encoded data to generate a plurality of partially decoded data streams) (emphasis added); *see also* '700 Patent, Claim 15 at 12:27-30 *and* Ex. A at 10. Because the claimed invention is complex and involves distinct circuit components, it is insufficient for ViaSat to stretch *one* signal diagram, probed from *one* location, to support *three* limitations at different locations in the circuit, especially where ViaSat characterized two of those limitations as points of novelty.

IV. CONCLUSION

For the foregoing reasons, ViaSat fails to plausibly allege infringement under heightened or even standard pleading requirements. Despite asserting technologically complex and purportedly novel claim limitations, ViaSat supports those limitations insufficiently and inconsistently. Accordingly, this Court should dismiss ViaSat's complaint.

[5] ViaSat cannot argue that the relevant decoder is included with the flash memory because it repeatedly asserts that the *controller* rather than the flash memory includes the relevant decoder. *See* Compl. ¶¶ 50, 56, 57, and 59.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that all counsel of record who are deemed to have consented to electronic service are being served April 1, 2022, with a copy of this document via the Court's CM/ECF system.

/s/ *Robinson Vu*
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